

SEMICONDUCTOR MEMORY COMPONENT

5 Cross-Reference to Related Application:

This application is a continuation of copending International Application No. PCT/DE02/01504, filed April 24, 2002, which designated the United States and which was not published in English.

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Background of the Invention:

Field of the Invention:

The invention lies in the semiconductor technology and memory technology field. More specifically, the invention relates to
15 a semiconductor memory component. In such components, a semiconductor memory is produced on a chip as a configuration of memory cells. An integrated circuit allows the semiconductor memory to be used, in particular the individual memory cells to be addressed. Electrically conductive
20 connections in the form of word lines and bit lines set up the connection between the connections provided for actuating the memory cells and the memory cells and are provided for programming the memory cells. Programming and reprogramming the memory cells store digital information in the cells in the
25 form of logic 0 or logic 1. The information is read in a prescribed manner when the memory cells are addressed.

The stored data are input and output, and the control signals provided for addressing or for generally controlling use of the memory are input, in the form of digital input signals and
5 output signals. Since the information content of the individual bit is extremely small, a multiplicity of such signals need to be transmitted in parallel or serially. Ordinary semiconductor memory chips are therefore provided with a very large number of connection contacts. This results
10 in high costs for the packages in which the semiconductor memory chips are mounted.

Such a package comprises, by way of example, a patterned metal support which likewise holds a corresponding number of
15 connection contacts. These contacts need to be connected in pairs to the corresponding contacts on the memory chip. Since each data output is able to output just one value at any time, this results only a low data rate.

20 When the memory cells are arranged in the semiconductor memory in matrix form, the bit lines and word lines need to be used to address the rows and columns in this memory cell matrix at offset times. This results in long access times. The number of connection contact areas required therefore rises very sharply
25 as the size of the memory increases. The latter, however, is the object of the progressing technology. By limiting the

possible number of connection contacts, the capacity limit of the memory chip is reached very quickly.

Summary of the Invention:

5 It is accordingly an object of the invention to provide a semiconductor memory component, which overcomes the above-mentioned disadvantages of the heretofore-known devices and methods of this general type and which provides for a semiconductor memory component with short access times or high
10 data rates even when the memory capacity is high.

With the foregoing and other objects in view there is provided, in accordance with the invention, a semiconductor component with a semiconductor chip that has a semiconductor
15 memory with a memory array of a plurality of memory cells. The device has:

at least one connection contact;

an electrically conductive connection between the at least one connection contact and the semiconductor memory;

20 at least one converter device selected from the group consisting of a digital-analog converter and an analog-digital converter incorporated in the electrically conductive connection for enabling a utilization of the semiconductor memory with analog signals; and

wherein a number of the connection contacts for the semiconductor chip is less than a number of connection contacts required for a utilization of the semiconductor memory with digital signals.

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In other words, the inventive component is provided with at least one digital-analog converter and/or at least one analog-digital converter, specifically preferably a plurality of such converters, which are incorporated into the electrically
10 conductive connections between the connection contacts and the memory cells such that it is possible to use the semiconductor memory by inputting or outputting analog signals. The analog signals are equivalent to superimposition of a multiplicity of digital signals.

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If analog outputs are provided instead of the previous digital outputs in a semiconductor memory, therefore, the same volume of data, for which a plurality of connection contact areas (pads) were normally required, can be read via just one
20 connection contact. The data can be written in by inputting the data in the form of analog signals and using an analog-digital converter to convert them into a plurality of digital signals, which are forwarded in an ordinary 16-bit bus, for example.

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The same principle can also be applied to addressing the memory cells. In this regard, the connection contact areas for inputting the addressing signals are replaced by a smaller number of connection contact areas, particularly two contact areas for the row address and the column address, and analog-digital converters are provided behind them for the purpose of converting the analog control signals which are input on the connection contact areas into digital addressing signals. This component therefore saves a very large number of connection contact areas on the semiconductor chip, and also on the package, in particular. In addition, a faster interface is obtained for the data and addresses.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in a semiconductor memory component, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description

of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

5 Figs. 1 and 2 are diagrams showing two connection schemes for semiconductor memories in the prior art; and

Figs. 3 to 5 are similar views showing corresponding connection schemes for examples of the component in accordance
10 with the invention.

Description of the Preferred Embodiments:

Referring now to the figures of the drawing in detail and first, particularly, to Fig. 1 thereof, there is shown an
15 exemplary component with a connection scheme in which, on the basis of the prior art, a semiconductor memory 1, in this case an FIFO memory, is connected to connection contact areas 3 via an ordinary 16-bit data line 2. The connection contact areas can be used for tapping off the digital data transmitted in
20 parallel when the memory 1 is read.

Fig. 2 shows a corresponding scheme for addressing the semiconductor memory based on the prior art. In this case, addressing latches 40 are shown which are controlled via an
25 address bus 50 with the digital signals that are input on the connection contact areas 3. The connection contact areas

(address pads) have a row address and then a strobe signal (row address strobe) applied to them, as a result of which the row address is stored in the latches. The column address is then applied to the same connection contact areas 3. A strobe
5 signal (column address strobe) is applied again, as a result of which the column address is stored in the latches.

Fig. 3 shows a scheme, corresponding to that in Fig. 1, according to which a component in accordance with the
10 invention allows the memory content to be read. The semiconductor memory 1 has a multiplicity of data lines coming from it, in the form of 16-bit data lines 2 in the exemplary illustration. Instead of being routed directly to the connection contact area 3, the data lines incorporate a
15 digital-analog converter 6 which converts the digital signals into an analog signal. This analog signal can be tapped off on a common connection contact area 3.

If certain exemplary embodiments of the component do not allow
20 all the signals on a 16-bit data bus to be superimposed to form an analog signal, it is also possible for a plurality of connection contact areas 3 to be provided which are supplied with a respective analog signal formed from partial
superimposition of the digital signals. In addition, the use
25 of parallel data buses for the converted, analog signals allows faster transmission of the data.

The inventive memory component is addressed in the manner shown by the scheme shown in Fig. 4. In this example, just one respective connection contact area is provided for row
5 addressing and column addressing. These contact areas can have the analog control signals applied to them, which are each subsequently converted in an analog-digital converter 7 into the digital signals, which are supplied to the address latches 4 via a respective address bus 5.

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Fig. 5 shows a further exemplary embodiment using a scheme corresponding to that in Fig. 3. This exemplary embodiment illustrates that a plurality of 16-bit data buses 20, 21, of which two are shown in this case, can be converted in parallel
15 into analog signals using digital-analog converters 60, 61, said analog signals being supplied to the connection contact areas 3. This means that it is possible to transmit an even greater number of data in parallel without the number of connection contact areas 3 exceeding a tolerable limit.

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The inventive component can be in a form such that read and write operations are possible by outputting and inputting analog data. Instead of the data which are to be stored or are stored, it is also possible to transmit control signals for
25 controlling read and write operations, particularly for

addressing memory locations, by inputting analog control signals.

In one preferred refinement of the component, both, i.e. the
5 read and write operations and control thereof, are performed
exclusively by inputting and outputting analog signals. In
this refinement, communication with a memory controller is
therefore effected exclusively using analog signals.

10 If a plurality of connection contact areas are provided for
data input and data output, the transmitted data rates can be
significantly increased. With a connection contact area and a
16-bit digital-analog converter, for example, 16 bits per
clock cycle can be transmitted during a read operation; the
15 same data rate is achieved with two 8-bit digital-analog
converters and two connection contact areas. By using digital-
analog converters of suitable capacity and a sufficiently
large number of connection contact areas, much higher data
rates can therefore be transmitted as compared with
20 conventional memory components.

In this case, conversion between digital and analog signals is
respectively performed such that the relevant information is
retained. The number of digital signals which is superimposed
25 to form analog signals must therefore possibly be subject to
appropriate restriction for certain applications of the

inventive component. Since it is possible to convert a plurality of digital signals into an analog signal or to convert an analog signal into a plurality of digital signals in all cases, however, it is possible to save a large number
5 of connection contact areas with the inventive memory component in any exemplary embodiment.